

Systems of Chiplets

The Coming Wave

Will Chiplets Be the Next Wave for our Industry's Scaling?

The 80's Revolution

- Enabled logic designers to create chips



Logic designer



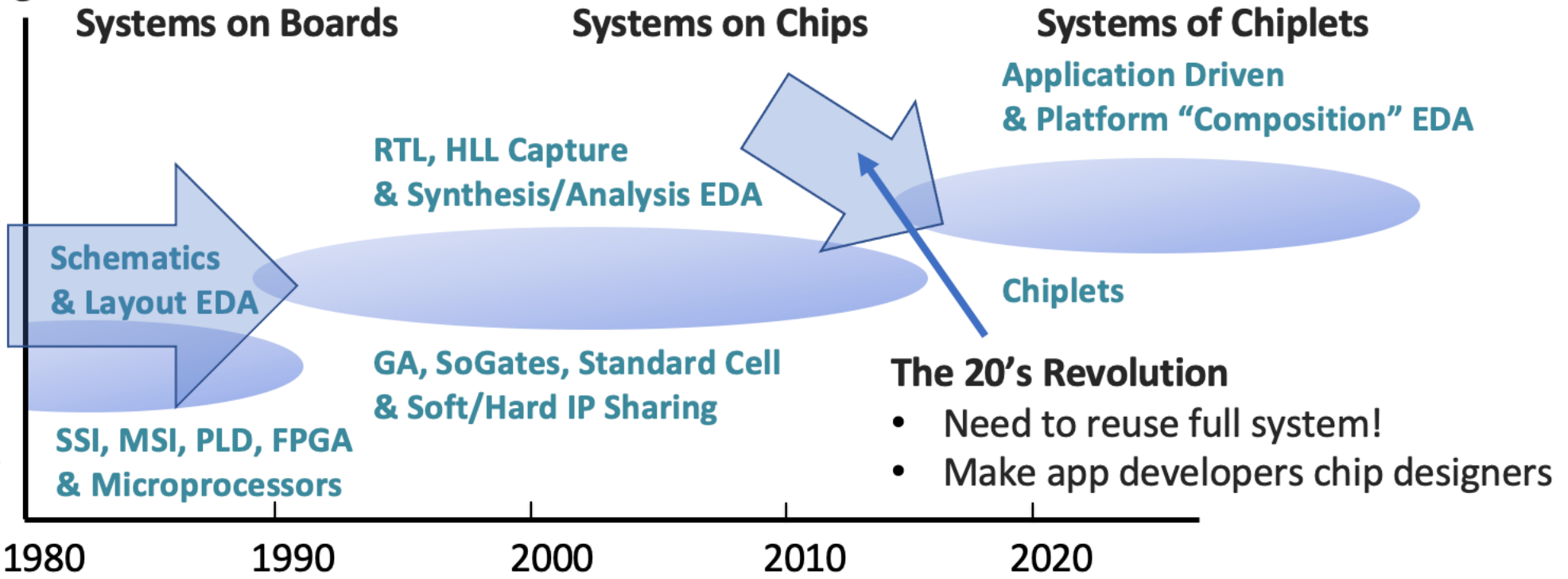
IC designer

The Coming Third Wave

Systems on Boards

Systems on Chips

Systems of Chiplets



The 20's Revolution

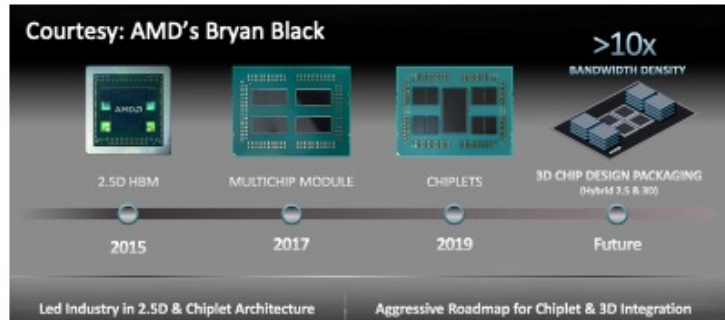
- Need to reuse full system!
- Make app developers chip designers

On the Spectrum

Industry Plan

The road well traveled

- Use chiplets for HV apps
- To create needed SKUs



Opportunity Missed

Industry will miss a lot



Democratizing Design

The road less traveled

- Enable app designers to create chips
- By creating an app API for chiplets
- Focus on accessibility, not performance

Our Panel



Dr. Bryan Black

CEO, Chiptetz



Bob Brennan

VP & GM, Intel
Foundry Services



Prof. Bill Dally

Chief Scientist & SrVP
Research, Nvidia

Professor, Stanford



Liam Madden

Adjunct Prof &
SystemX Alliance
Director, Stanford



Dr. Ming Zhang

Distinguished
Architect, Silicon
Realization,
Synopsys

Panel Strategy

First perspectives ...

You've just heard from Bryan. I'll introduce each other panelist and they'll (briefly) share their perspectives.

Second some opening questions ...

To start things off, I'll fire off 1 question for each panelist to begin.

Open season ...

We'll just just open the floor to questioning, if it hasn't already begun.

Panel Time: 2:00 – 2:45

BIOS

Dr. Bryan Black

- CEO & Co-Founder, Chiptetz
- Formerly Senior Fellow at AMD ('07-'21), Intel ('00-'07)
- At AMD, Bryan led the technology developments leading to the multi-chip module and stacked die products across the company's portfolio, including the design of high-bandwidth memory (HBM) and its first implementation in the "Fiji" GPU.
- His work forms the foundation for many of today's system-in-package implementations for AI and high-performance computing across the industry.
- BS, MS and PhD in Computer Engineering @ Carnegie Mellon University

Bob Brennan

- VP/GM, Intel Foundry Services, Customer Solutions Engineering Intel
- Formerly Micron ('18-'21), Samsung ('13-'18) & Intel ('91-'13, 21 years!)
- Responsible at Intel for the delivery of end-to-end design “customer” solutions. This covers the entire design life cycle for customers, from customer design architecture to the strategic selection of Intel IP to platform enablement, as well as design services support for SoC integration including validation and debug support.
- At Micron, Bob served as Vice President of Emerging Memory & System at Micron, where he managed product, design, and engineering teams to accelerate the delivery of new designs on new technologies.
- At Samsung, Bob was Senior Vice President of Memory Solutions Lab, where he established an Enterprise SSD product line, delivered Samsung’s first revenue software product while continuing an active role in architecture development.
- Prior to these roles, Bob spent 22 years at Intel serving in various senior technical positions, including Server Architecture, Laptop Architecture, Mobile SoC Architecture, and CPU Core Design, Verification and Architecture.
- BSEE @ Duke, MSEE @ Univ of Virginia

Prof. Bill Dally

- Professor & former CS department chair, Stanford University
- Chief Scientist & SrVP Research, Nvidia
- Member of the President's Council of Advisors on Science & Technology
- Professor, MIT ('86-'97)
- Research focus on most every aspect of parallel machines
- National Academy of Engineering, a Fellow of the American Academy of Arts & Sciences, a Fellow of the IEEE and the ACM, and has received the ACM Eckert-Mauchly Award, the IEEE Seymour Cray Award, and the ACM Maurice Wilkes award
- BSEE @ Virginia Tech, MSEE @ Stanford & PhD @ Caltech
- Cofounder of Velio Communications and Stream Processors
- Pilot

Liam Madden

- Stanford SystemX Alliance, Technical Director
- Adjunct Prof, Stanford & Adjunct Prof, Univ College Dublin
- Formerly Xilinx ('08-'22), AMD ('06-'08), Microsoft ('03-'05), MIPS ('96-'03) & DEC ('84-'96)
- At Xilinx, Liam was last the ExecVP & GM for the Wired and Wireless Group. His prior responsibilities there included the development of the highly successful 28nm, 20nm and 16nm All Programmable families. Specifically, he was responsible for the introduction of stacking technology at 28nm, leading the industry in integrating multiple devices on a Silicon Interposer for which he received the 2013 Semi Award.
- In over a 35 year career he contributed to a range of industry leading products, including: high performance and low power microprocessors (Alpha and StrongArm at DEC), embedded processors and IP (MIPS) and consumer devices (Xbox 360 at Microsoft). Prior to joining Xilinx, he was a Senior Fellow at AMD, where he drove AMD's next generation chip integration methodology.
- B of Eng @ UCD, M of Eng, Cornell

Dr. Ming Zhang

- Distinguished Architect, Silicon Realization Group, Synopsys
- Active advisor & mentor for Prime Movers, Activate, Skydeck and StartX
- Formerly CEO & Co-Founder of Zglue ('14-'20), “The chiplet company for the rest of us”
- Formerly also Samsung ('10-'11, '13-'14)), Intel ('06-'10) and a number of startups
- At Synopsys, Ming is responsible for technology strategy and market development for Silicon Realization Group (SRG) product portfolio. That group is the home of design and verification software platforms at Synopsys. SRG is a customer-first team that constantly pushes the boundaries of innovation in diverse EDA areas like simulation, static analysis, debug, formal, synthesis, P&R, signoff, power, test, silicon lifecycle management, and 3DIC.
- BS Physics @ Peking University, MS EE and PhD EE from Univ of Ill, Urbana