Open Architectures to Accelerate Industry Growth

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Moore’s Predicted “Day of Reckoning”

“It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected.”

-Gordon E. Moore

1: “Cramming more components onto integrated circuits”, Electronics, Volume 38, Number 8, April 19, 1965
System on Chip -> System of Chips

“Catalyzing the Impossible: Silicon, Software, and Smarts for the SysMoore Era” – Dr. Aart de Geus

Google Cloud Blog*: A Chiplet Innovation Ecosystem for a New Era of Custom Silicon

What’s needed:

• Modularity
• Optimized Silicon and Package
• Open Standards, examples:
  ▪ IO
  ▪ Protocols
  ▪ Security
  ▪ Management

Growing Demand for AI

Growing Demand for Video

(YouTube, Live Streaming)

*https://cloud.google.com/blog/topics/systems/open-chiplet-ecosystem-powering-next-era-of-custom-silicon
Intel® Vision: The “Chiplet Revolution”

Open Chiplet: Platform on a Package

- Customer IP and Customized Chiplets
- High-Speed Standardized Chip-to-Chip Interface (UCIe)
- 20X I/O Performance at 1/20th Power*
- Advanced 3D Packaging

*relative to PCIe G5 x16
Motivation: Cost & Manufacturing Optimization

Monolithic Chiplet

300 mm²

79-83 mm² ea.

Input Variables:
- Die Area
- # of Chiplets
- Wafer Cost
- Defect Density
- Package/Assembly/Test
- Known Good Die
- Die Area Tax & Overhead

"Heterogeneous Integration of Chiplets: Cost and Yield Tradeoff Analysis"

Source: Intel® Model

*Probabilistic trend by 1std dev
Motivation: Process Technology Optimization

- Logic/Memory
- IO
- RF
- Mixed-signal

Source: Intel®

Density
Leakage
Speed
High-Voltage
Passive

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Motivation: AI Memory BW/Power Gap

- Insatiable Memory Bandwidth
- The energy efficiency gap is getting bigger

Source: Intel®
Motivation: R&D Cost and Product Velocity

Move from Exponential -> Linear with modularity and reuse
Motivation: Optimize System Level High Speed IO

Source: Intel®
Technology Needed

Some EDA Challenges
New Development Model: System on Chip -> System of Chips

- Platform & SW/HW Co-Design
- Architecture Perf. Modeling
- RTL Design & Verification
- Synthesis
- Auto Place & Route (APR)
- Mask Set
- First Silicon
- Shipped Products

Architecture

IP/SOC Design

System Lifecycle Management

Post-Si & Test
Architecture: Optimal Silicon Partitioning

Comparative/pairwise analysis for any homogeneous or heterogeneous implementations
Shifting Left with SW/HW Co-Design

SoC Development

Virtual Prototyping

Emulation

Prototyping

Incremental Approach

SW Development

Save 3 - 6 months

Shift Left

Source: Synopsys
Shifting Left with SW/HW Co-Design
Ex. Intel® Simics® Virtual Platforms

System Level Features Support
- Scripting
  ```bash
  $ foo
  $ bar
  ```
- Fault injection & control
- Matches hardware functionality
- Multicore & -machine multithreading
- Modular & user-extensible

Real-world Connections
- Mouse, keyboard, serial, network, PCIe

Integration of 3rd party entities
- External SW Tools
  - Intel System Debugger, GDB, WinDBG, Lauterbach, ...
- Other Simulators
  - VCS, Cadence, Synopsys, Matlab, C, ...
- RTL Emulation / FPGA
  - Synopsys HAPS & ZeBu, Intel® systems, ...

Simics®
Architecture: System of Chips Performance Modeling
Ex. Intel® CoFluent™ Technology

Execute real SW workloads

Shape Micro-architectural details
Architecture: System Power & Thermal Optimization

Ex. Intel® Docea™ – System Thermal Analysis -> Quick Iteration (Arch, Design, Power, Thermal)
Design: Standardized IP: HIP and SIP

Ex. UCle Open Interconnect

**INITIAL FOCUS**

- Physical Layer: Die-to-Die I/O with industry leading KPIs
- Protocol: CXL/PCIe for near-term volume attach
- Well-defined specification: ensure interoperability & evolution

**FUTURE GOALS**

- Additional protocols (ex. CHI)
- Advanced chiplet form-factors
- Chiplet management
- Security
- And much more!
Design: DTCO & STCO Silicon + Package

PPAC Silicon Optimization, Package-Silicon Optimization

Foveros Omni enables flexible design with maximum performance

- TSV penalty minimized
- Power and IO optimization
- High bandwidth interconnects

Foveros Direct direct copper-to-copper bonding which enables low resistance interconnects

- Bump density increases to 30K/mm²
- Functional block level partitioning

Test wafer with Foveros Omni
Design: Power Delivery

Power to the Platform – clean & efficient

Distributed Power Delivery Droop

Optimize Voltage Regulators

Distribute Power Delivery

Optimized
Power Management IC (PMIC)
Post-Si: Platform Validation and Debug

New Post Silicon Multi-Die Tools/Flows/Methods, new Design for Debug Architecture
Post-Si: Manufacturing and Test

New Test Architecture & Capabilities: Known Good Die -> Known Good Multi-Die
Test & Life Cycle Management

**Implementation**
- DFT Logic

**Data Acquisition**
- Scan chain results

**Data Export**
- Scan shift, JTAG, USB, PCIe

**Analytics**
- Scan diagnostics

<table>
<thead>
<tr>
<th>Test</th>
<th>System Lifecycle Management</th>
</tr>
</thead>
<tbody>
<tr>
<td>DFT Logic</td>
<td>Embedded In-Chip Monitors</td>
</tr>
<tr>
<td>Scan chain results</td>
<td>Process, Voltage, Temperature &amp; Path Margin</td>
</tr>
<tr>
<td>Scan shift, JTAG, USB, PCIe</td>
<td>iJTAG, JTAG, Scan, USB PCIe, CPU</td>
</tr>
<tr>
<td>Scan diagnostics</td>
<td>Manufacturing reporting and production control</td>
</tr>
</tbody>
</table>

Source: Synopsys

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Chiplets

Industry Case Studies & Representative Applications
Case Study: Intel® Client, Lakefield 3D Foveros

Ex. Market Segmentation (GFX, Memory), Process Optimization

<table>
<thead>
<tr>
<th>Y SKU Gen-1</th>
<th>Y SKU</th>
<th>LKF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package</td>
<td>20.5x16.5</td>
<td>26.5x18.5</td>
</tr>
<tr>
<td>Memory</td>
<td>LP3 11x11.5</td>
<td>LP4-4x 12.5x12.5</td>
</tr>
</tbody>
</table>
Case Study: Intel® HPC - Ponte Vecchio

Ex. Complexity Management, Process Optimization
IO Optimization: Intel® Optical

Ex. Network Optimization through Modularity
Sensor Case Study: Radar Beamforming Application
IO Case Study: Disaggregated PCIe & Memory

Ex. Optimization of Process (ex. Analog), Supply Chain
IO Case Study: Possible HBM Architecture

Optimize: AI Bandwidth/Power Density, AI Thermals
Server Case Study: Multi-core uServer

Ex. Multi-Protocol Architecture: CXL/UCie and CHI/UCie
Networking/Storage Case Study: IPU/DPU

Ex. Multi-Protocol Architecture: AXI/UCie; Networking Modularity

- AXI/UCie
- Network On Chip (AXI)
- Shared Cache
- RDMA/CXL Ethernet
- ETHERNET 224G
  - Copper
  - Optical

- Manageability & Security
- CPU Sub-system (8–64 core)
- Storage Accelerators

- RISC-V arm
AI Case Study: Caching Inference Architecture

Ex. DMA, Asymmetric Coherence, Symmetric Coherence

- CXL.IO
- CXL Cache
- Fully Symmetric Cache

Scheduler

Execution Core

AI | Stream Processors

- Instruction Cache
- Data Cache

L2 Cache

L3 Cache

DDR5 or LPDDR5

UCle

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Summary

- Industry Vision – we are at an inflection point
- Technical Challenges – die size, process, IO, and R&D $ optimization
- Technology Needed – RISC-V open architecture, new CAD tools in Architecture, Design, and Debug & Test
- Commercial Case Studies – many new emerging architectures, it’s just the beginning, let’s collaborate!
Thank you