Chiplets

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Why Chiplets - or for the over 40’s MCM’s?

• We built MCM’s when we couldn’t afford to build a monolithic device

  DEC PDP-11 (J11) circa 1982
  Package ~79mm x 36mm, Ceramic
  4um CMOS (Harris), 2 Die
  ~120K Transistors

• We still do!

  Xilinx VU19 circa 2021 (First products ~ 2011)
  Package 65mm x 65mm, Organic with CoWoS Silicon Interposer
  16nm CMOS (TSMC), 4 Die
  ~35B Transistors
Why Chiplets?

• We also built them when we needed to mix technologies and maximize bandwidth

ATI Xenos GPU + EDRAM (XBOX 360) circa 2006
Package Organic
GPU, 90nm TSMC
EDRAM, 90nm NEC

• We still do!

Xilinx/AMD Versal HBM, 2021
Package Organic with CoWoS Silicon Interposer
FPGA, 7nm TSMC
HBM2e memory stack
But not all products benefit

• Shannon Test Chip (early poster child for mixed digital/analog + IP reuse)
  
  Xilinx ~ 2013
  Package Organic, 35mm x 35mm with CoWoS interposer
  FPGA, 2 x 28nm TSMC (reused)
  16xDAC and 16xADC, 65nm TSMC
  
  Cost challenged due to Interposer + Assembly costs
  Re-used die did not have processor (originally optimized for wired comms)

  A Heterogeneous 3D-IC consisting of two 28nm FPGA die and 32 reconfigurable high-performance data converters, ISSCC 2014

• RFSOC Product
  
  Xilinx ~ 2016
  Package Organic, 35mm x 35mm
  FPGA +CPU+ 16xDAC + 16xADC, 16nm TSMC Monolithic

  A modular 16NM Direct-RF TX/RX Embedding 9GS/S DAC and 4.5GS/S ADC with 90DB Isolation and Sub-80PS Channel Alignment for Monolithic Integration in 5G Base-Station SoC, IEEE Symposium on VLSI Circuits 2018
Takeaways

• Some chiplet cases are easy to justify:
  • Larger than reticle or high margin/bandwidth heterogeneous designs (e.g. HBM)
• For other designs...it’s complicated (even AMD ships monolithic CPU’s)
• Cost of Goods Sold (COGS) and Gross Margin (GM) are the primary impediments (GM=Revenue-COGS, GM%=1-COGS/Revenue)
  • COGS for smaller chips can be dominated by:
    • Package/interposer/silicon bridge and their assembly cost
    • Added area for interfaces
    • Extra cost at wafer test to reduce final test fallout (which is multiplicative)
• Wall Street abhors reduced GM - who will lose on margin stacking for multi-sourced die?
  • Lower product development cost has never been a good argument with customers if their ASP increases due to stacking