AHA: An Agile Approach to the Design of Programmable Accelerators and Compilers

Priyanka Raina
Assistant Professor of Electrical Engineering
Stanford University
praina@stanford.edu

August 25, 2022

Day 2 Agenda

Session 1: Domain-Specialized Hardware Accelerators

9:10 – 9:35	Amber: Coarse-Grained Reconfigurable Array-Based SoC for Dense Linear Algebra Acceleration Alex Carsello
9:35 – 9:50	Amber Demo Kathleen Feng
9:50 – 10:15	Onyx: A 12nm SoC with a Coarse-Grained Reconfigurable Array Accelerating Dense and Sparse Applications Kalhan Koul
10:15 – 10:35	Break

Day 2 Agenda

Session 2: Compilers and Hardware Design Tools

10:35 - 11:00	The Sparse Abstract Machine Olivia Hsu
11:00 - 11:15	Bringing Software-Style Linking and Interoperability to Hardware Development Ross Daly
11:15 - 11:30	Bringing Source-Level Debugging Frameworks to Hardware Generators Keyi Zhang
11:30 - 11:45	Breaking Down Physical Design Barriers with Open and Agile Flow Tools (A Perspective from DAC'22) Chris Torng
11:45 - 12:00	Software Systems for Mixed-Signal Hardware Sara Achour
12:00 - 1:30	Lunch

Day 2 Agenda

	Session 3: Chiplet Ecosystem for Agile System Design
1:30 - 2:00	Keynote 1 - The Package is the System Bryan Black
2:00 - 2:45	Chiplet Panel Discussion Bob Brennan, Bill Dally, Liam Madden, Ming Zhang, Bryan Black
2:45 - 3:15	Break
	Session 4: Future of AI Applications
3:15 - 3:45	Keynote 2 - A Kaleidoscope of Butterflies: Structured, Hardware-Friendly Sparsity in High-Throughput ML Training Christopher Ré
3:45 - 4:00	The Future of Sparsity in Deep Neural Networks Trevor Gale
4:00 - 4:15	System Design for AR/VR Ron Ho
4:15 - 4:45	Closing Thoughts & Wrap-up Discussion