AHA: Agile Hardware-Compiler Co-design and Verification

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August 31, 2023

Day 2 Agenda

9:15	**Pushing the Limits of Scaling Laws in the Age of Large Language Models** Azalia Mirhoseini
10:00	**Onyx: A Coarse-Grained Reconfigurable Array for Accelerating Dense and Sparse Tensor Algebra** Kalhan Koul
10:20	Break
10:50	**Cascade: An Application Pipelining Toolkit for Coarse-Grained Reconfigurable Arrays** Jackson Melchert
11:10	**Efficiently Synthesizing Lowest Cost Rewrite Rules for Instruction Selection** Ross Daly
11:30	**Lightweight Online Learning for Bounded Model Checking** Andrew Wu
11:50	Lunch

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13:20	**Energy Efficiency and AI Hardware** Bill Dally
14:05	**Sparse PyTorch** Bobby Yan
14:25	**Sparse Recurrences and Linear Solvers** Shiv Sundram
14:45	**ASPEN: Acceleration of Visual Inertial Odometry for Extended Reality on an FPGA** Kathleen Feng
15:05	Break

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15:35	**Learnings from Edge AI Chip Designs with Applications in Probabilistic and NLP Inference and Training** Thierry Tambe
15:55	**Interrupt-Driven Viterbi for High-Speed Links** Zachary Myers
16:15	**Avanergy: An Architecture-VLSI Abstraction for Automated Energy-Aware Design-Space Exploration Tools** Christopher Torng
16:35	**Wrap-up Discussion & Closing Thoughts** Priyanka Raina