Summary of the PCAST Report on Revitalizing the U.S. Semiconductor Ecosystem

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Revitalizing the U.S. Semiconductor Ecosystem

- Report prepared by PCAST Working Group on Semiconductors to advise the President on how to invest the R&D funding in the CHIPS and Science Act
    - **$11 billion** over **5 years** in semiconductor **R&D**

- https://www.whitehouse.gov/wp-content/uploads/2022/09/PCAST_Semiconductors-Report_Sep2022.pdf

PCAST Working Group on Semiconductors

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Recommendations

1. The Secretary of Commerce should establish **NSTC** as an independent legal entity in **public-private partnership** by the **end of 2023**. The Secretary of Commerce should select a Board of Directors, and that Board should oversee both the NSTC and the NAPMP to ensure synergy and alignment in the investments. The Board members should include **broad representation from government, industry, and academia**.

2. The Secretary of Commerce should ensure that the NSTC founding charter includes **establishing prototyping capabilities** in a geographically distributed model encompassing up to **six coalitions of excellence (COEs)** aligned around major technical thrusts such as advanced logic; advanced memory; analog and mixed-signal; life science applications; design and methodologies; and packaging. The packaging COE should encompass the budget and the objectives of the NAPMP initiatives.

Recommendations

Workforce Focused Recommendations

3. The Secretary of Commerce in coordination with the Director of the National Science Foundation (NSF) should support the establishment of a **national microelectronics education and training network** by the end of 2023 and allocate funding on the order of **$1 billion** over the next 5 years to upgrade educational laboratory facilities, support curriculum development, and facilitate hiring of faculty into this field.

4. The Secretary of Commerce should ensure that **NSTC-funded research supports** on the order of **2,500 scholarships and research assistantships per year** across the educational spectrum.

5. The Department of Homeland Security should implement existing statutory and regulatory authorities to provide premium processing to newly filed Immigrant Petitions for employment-based second preference advanced degree immigrants seeking a National Interest Waiver to work in microelectronics endeavors.

Recommendations

Startup Focused Recommendations

6. The Secretary of Commerce should ensure that by the end of 2023, the NSTC creates an **investment fund** on the order of **$500 million** to provide **financial support and in-kind access to prototyping and tools for semiconductor startups**.

7. The Secretary of Commerce should ensure that the NSTC **creates or funds the creation of a "chiplet" platform with a complete software stack** by the end of 2025 so that startups and academic institutions can integrate their custom chiplet(s) with the NSTC-supported chiplet platform **to demonstrate new innovations with dramatically reduced investment and time**.

Recommendations

Research Focused Recommendations

8. The Secretary of Commerce should ensure that the NSTC founding charter allocates a significant portion of the annual funding, on the order of **30 to 50 percent, to directly fund a national research agenda**. This research agenda should be broad in nature and address the following areas: **materials, process, and manufacturing technologies; packaging and interconnect technologies; energy-efficient computing and domain-specific accelerators; design automation tools and methods; semiconductor and system security; and semiconductors and life sciences**.

9. The NSTC should identify a set of **nationwide grand challenges** that are enabled through collaboration across the NSTC industrial membership and NSTC-funded research. These grand challenges should span **three complementary areas** that would benefit from large-scale nationwide collaboration: **advanced computing into the zettascale era; significantly reducing design complexity; and proliferating semiconductors in life sciences applications**.

Recommendations

10. To improve visibility into federal semiconductor investment efforts, measure the progress across the industry at the federal level, and maximize the leverage of such investments, we recommend the following:

    (a) Starting in 2023, and annually thereafter, the **NITRD** program should **collate and publish annual investment figures for semiconductors across all federal agencies**.

    (b) The NSTC should **encourage all agencies with semiconductor R&D investments to leverage and utilize the NSTC facilities and capabilities**. We recommend the NSTC **expand and co-fund programs with other agencies** and in public-private partnership where the research agendas are synergistic including, for example, **DARPA's Electronics Resurgence Initiative**, Research on the Future of Semiconductors sponsored by the **CISE Directorate at NSF**, and the broad multi-sector collaborations enabled by the **Semiconductor Research Corporation**.

    (c) The Secretary of Commerce should develop and regularly evaluate performance measures to **assess progress, effectiveness, outcomes, and impact of the CHIPS and Science Act initiatives** and report them annually to the President.

National Research Agenda

Six Coalitions of Excellence (COEs)	Research Directions
1. Advanced memory	1. Materials, Process, and Manufacturing Technologies
2. Advanced logic	
3. Packaging	2. Packaging and Interconnect
4. Emerging technologies including life sciences	3. Semiconductors and Life Sciences
5. Analog and mixed-signal	4. **Semiconductors and System Security**
6. **Architecture, design and tools**	5. **Energy-Efficient Computing and Domain-Specific Accelerators**
	6. **Design Automation Tools and Methodologies**

Energy-Efficient Computing and Domain-Specific Accelerators

- Domain-specific **accelerator architectures and design methodologies** that are more **resilient to fast-paced changes in algorithms** and applications
- Domains: **AI/ML (inference and training in the cloud and at the edge), graph analytics**, security, communications, bioinformatics, and optimization

- **Standardizing the interface** between the accelerator and the processor, memory system, and the rest of the system-on-a-chip

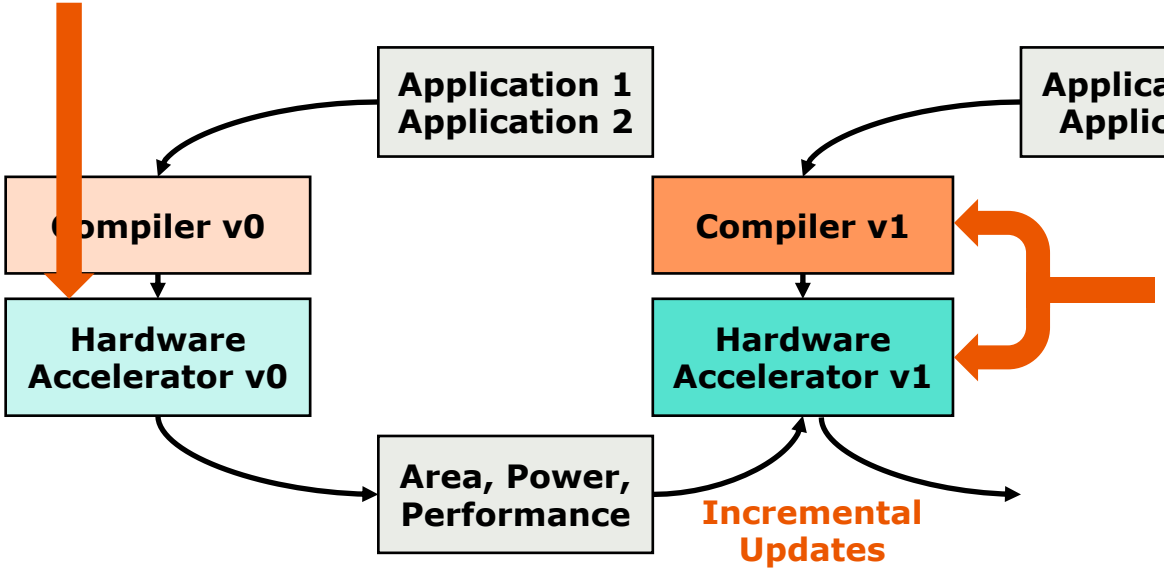
- Automate the **co-design of programmable accelerators and compilers**
- Comprehensive **software ecosystem** to make writing and executing new applications efficient and accessible for a wide range of accelerators

Design Automation Tools and Methodologies

- **Raising the level of design** so that chips and IPs can be compiled from high-level descriptions (above register-transfer level) much as software is compiled has the potential to greatly increase design productivity
- **Artificial intelligence** can be applied to every step of the design process to both **increase productivity and improve the quality of results**. Design tools, some based on artificial intelligence, can greatly **increase the productivity of analog, mixed-signal, and RF circuits** which are largely designed by hand today.
- **Emulation and virtual prototyping** technology that supports the verification of the exponentially growing complexity of both hardware and software is required for next-generation heterogeneous architectures

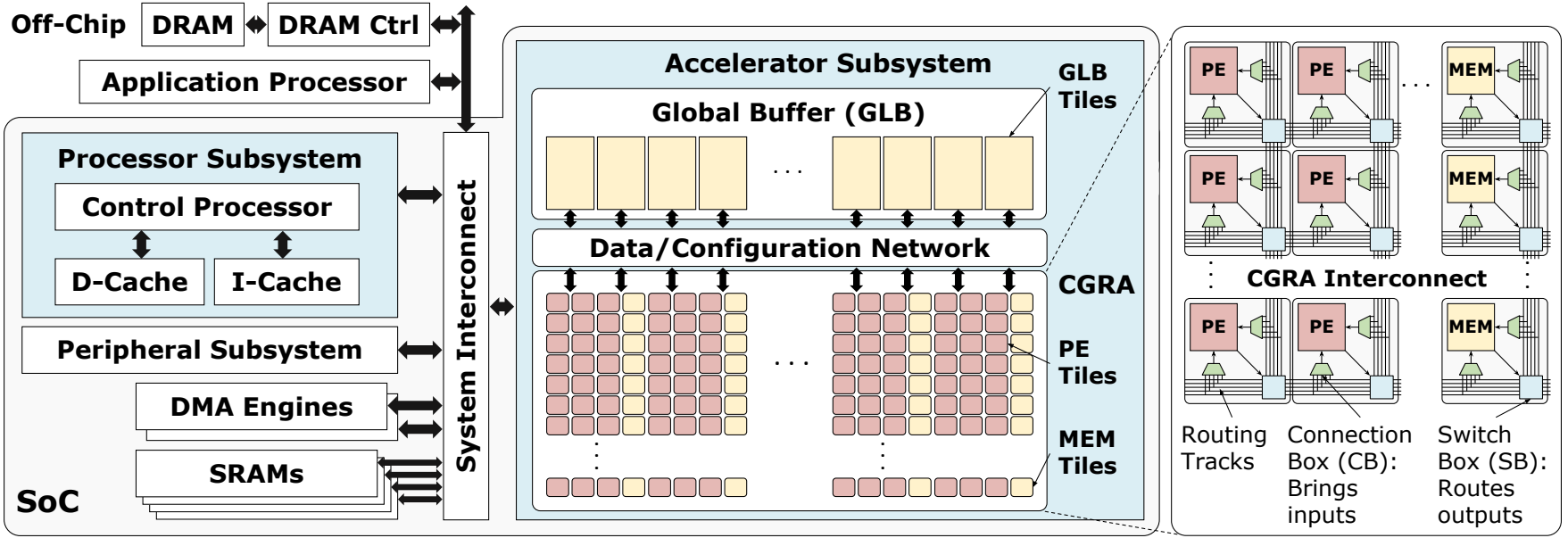
Agile Hardware-Software Co-design

1. Accelerator must be **configurable**
   So we can map new or modified applications to it (although with lower efficiency)

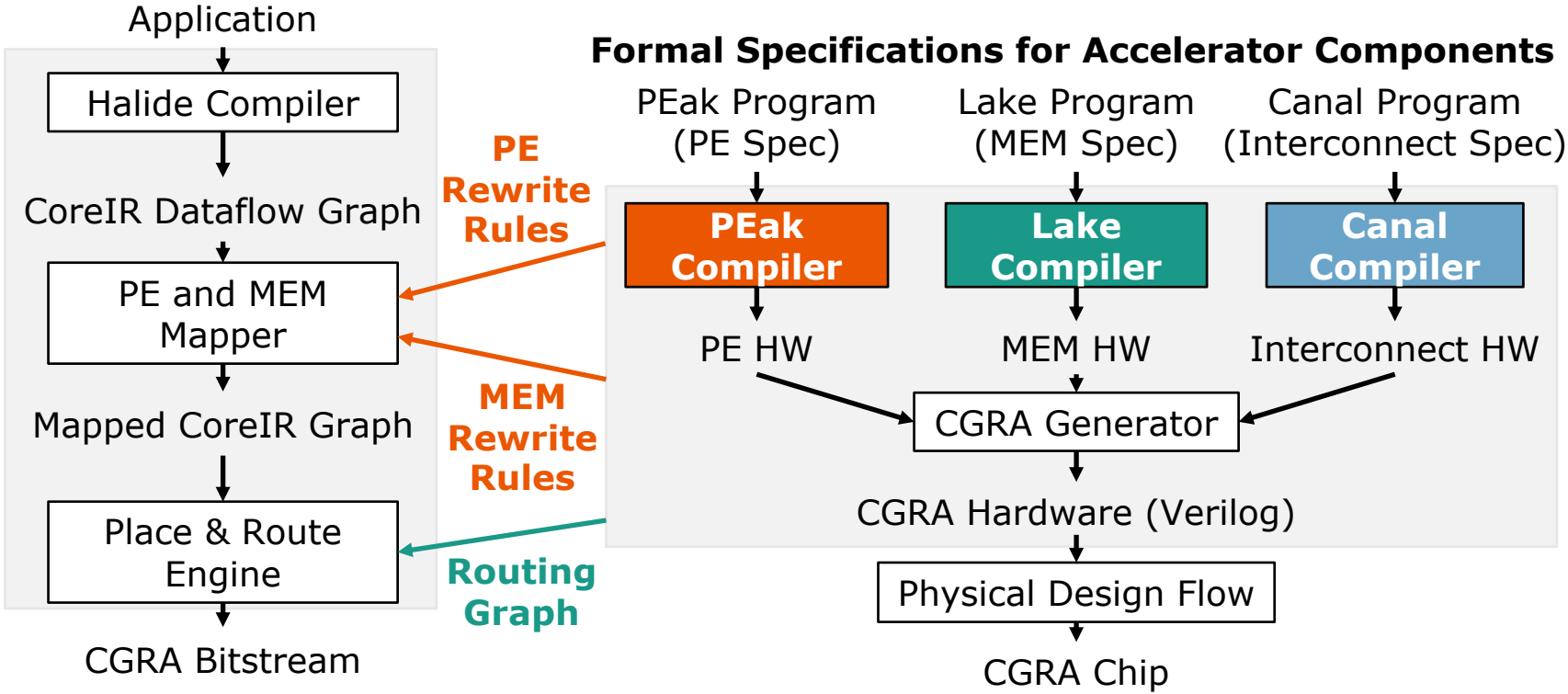


2. Hardware and compiler must **evolve together**
   - Any change in hardware must propagate to compiler automatically

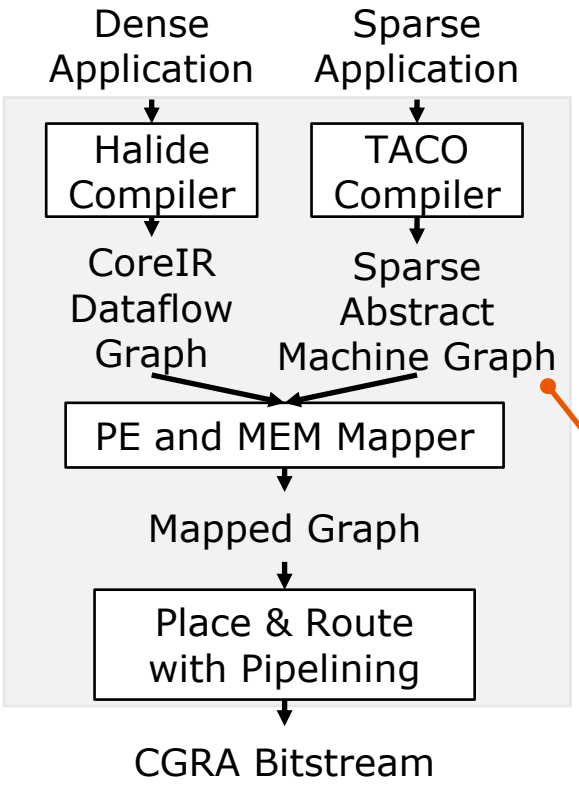
CGRAs as Accelerator Templates



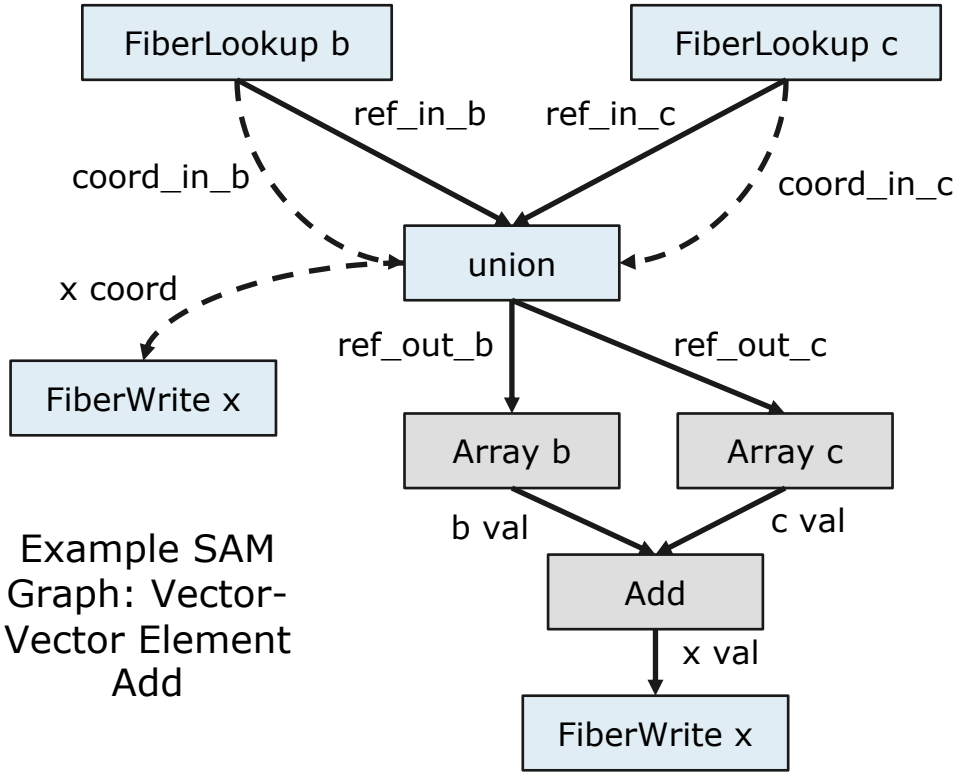
Automatically Generate HW and Compiler Collateral from a Single Source of Truth



Extending AHA to Sparse Applications



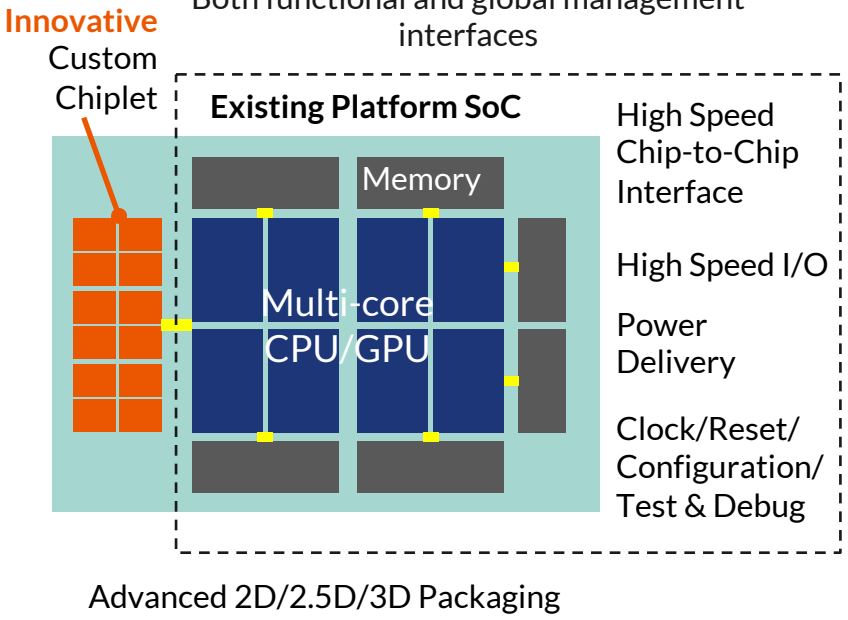
Example SAM Graph: Vector-Vector Element Add



Future Design Tools for Chiplet Based Systems

Need a **complete software stack for interaction** between the SoC and custom chiplet

Both functional and global management interfaces



Extend a base system, don't create a new system

Add an app to a system, through a supported API

Need to codify lots of IC design "know how"

Power, booting, testing, isolation, thermals…

Will require many new approaches, many will fail

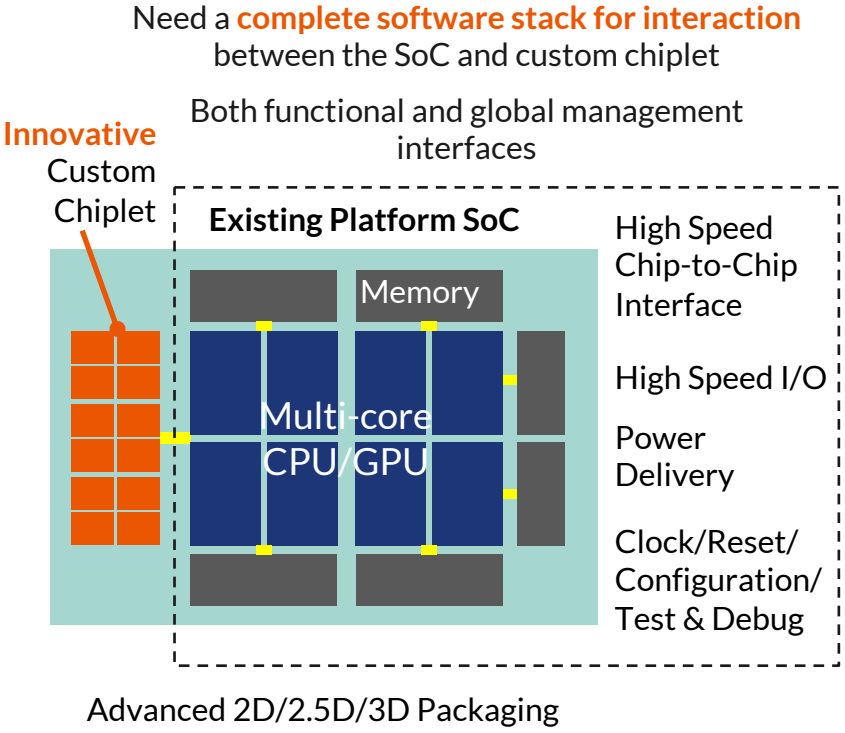
Enable new class of designers

People with app not hardware experience

Agile design tools meant for this audience

Focus is on productivity, not perfection

Future Design Tools for Chiplet Based Systems



Functional operation

Application API – how does user code access HW?

Includes memory model, DMA, config/control

Create plumbing to standard chiplet interfaces

And insert the right physical IP blocks into design

Platform integration

Encapsulated best practices for

- Debug of running system
- Testing / Isolation
- Initialization / Booting
- Thermals / Power

Research using APIs as high-level specs

- Tools then create implementations
- Formally checked

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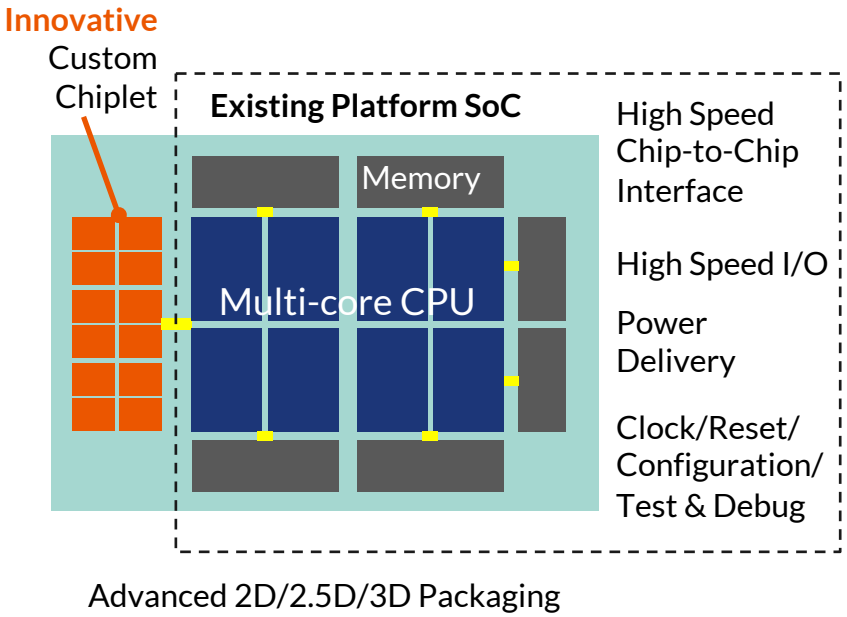

New center funded by Intel:

Heterogeneous Integrated Platforms (HIP) for 2.5D/3D Systems: App Store for Hardware

Base SoC + Chiplet version of our CGRA specialized for sparse machine learning