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SCALING PROVIDED A GREAT RIDE

For a 2x scaling
Get 4x more gates,
Gates get 2x faster,
Energy decrease 8x

Dennard, JSSC, pp. 256-268, Oct. 1974

No Exponential is Forever...but We Can Delay 'Forever', Moore ISSCC 2002
HOUSTON, WE HAVE A PROBLEM

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http://cpudb.stanford.edu/
TO CONTINUE TO SCALE PERFORMANCE

Apple’s A9 (2015)

https://www.anandtech.com/show/9686/the-apple-iphone-6s-and-iphone-6s-plus-review/3
HOW TO CREATE THESE ACCELERATORS?

• Study application
HOW TO CREATE THESE ACCELERATORS?

- Study application
- Design hardware
HOW TO CREATE THESE ACCELERATORS?

- Study application
- Design hardware
- Write software
NOT SO SECRET DOWNSIDE

$100M

Many Years
NOT SURPRISING

It is a waterfall model of design!

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SOFTWARE ISN’T BUILT THAT WAY

- Moved away from that style decades ago
- Enables small teams to build amazing apps
AGILE DESIGN

Rapidly iterate on end-to-end system

Learn about real problems, and goals
AHA!

Agile Hardware
AGILE DESIGN

It is about reuse

It is about clean interfaces

It is about constructors, not instances
PRODUCTIVITY IS THE ISSUE IN HARDWARE

Cost of Developing New Products

Source: IBS

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STILL NEED TO DEAL WITH FABRICATION

https://upload.wikimedia.org/wikipedia/commons/thumb/e/eb/12-inch_silicon_wafer.jpg/1024px-12-inch_silicon_wafer.jpg
NEED TO EVOLVE THE HARDWARE

- Use a CGRA – a configurable framework
AHA VISUAL COMPUTING

A new way to create DSSoCs

Compile → Evolves → Optimize

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FIRST GENERATION CGRA
APPLICATION COMPILATION FLOW

Halide

Var x, y, xi, yi, xo, yo; Func conv, out;
RDom win(0,3, 0,3);
kernel(x,y) = {{11,12,13},{14,15,16},{17,18,19}};
// algorithm
conv(x, y) += input(x+win.x, y+win.y) * 
            kernel(win.x, win.y);
out(x, y) = conv(x, y);
// schedule
conv.update(0).unroll(win.x).unroll(win.y);
out.tile(x,y, xo,yo, xi,yi, 62,62).reorder(xi,yi, xo,yo);
conv.linebuffer();

Compiler

CoreIR

Place & Route

Mapping

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MAINTAINING THE FLOW THROUGH CHANGES

- Many tools need to know about your design
  - You are building a “world”
DSSOC DOESN’T NEED TO BE EXPENSIVE

• One just needs to think about the problem differently

• We have already created one working chip/system using this flow

• And have the next generation of the system working

Stay Tuned for Future Results …